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(54) **Backup battery switch**

(57) A switching circuit for switching between a main power supply and a battery power supply includes a comparator, a p-channel battery power transfer transistor and an inverter. The comparator operates on the main power supply and is connected on input to the main power supply and to the battery power supply. The comparator compares the voltage level of the main power supply with the voltage level of the battery power supply and provides a selection signal which is low when the voltage level of the battery power supply is higher than the

voltage level of the main power supply. The p-channel battery power transfer transistor is controlled by the selection signal and transfers the battery supply signal to a switched power supply node. The inverter operates on the battery power supply and inverts the voltage level of the selection signal. The p-channel main power transfer transistor is controlled by the inverter and transfers the main power supply to the switched power supply node.

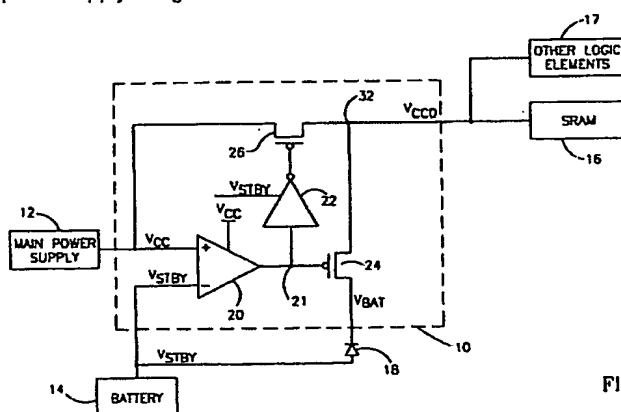


FIG. 1

Description

FIELD OF THE INVENTION

The present invention relates generally to circuits for switching between a main power supply and a backup battery power supply.

BACKGROUND OF THE INVENTION

Integrated circuits require a power supply to operate. When the circuit is not operating, the power supply is typically shut off. However, there are certain circuit elements for whom some level of power (such as battery power) is required at all times, even if the main power is shut down. For example, volatile random access memory (RAM) arrays, also known as "static RAMs" or SRAMs require some power to maintain the information stored therein, if such is necessary.

Power supply switches which select between a main power supply and a battery backup supply are well known in the art. These switches continually compare the voltage levels of the two supplies and switch to the battery supply when the voltage of the main power supply falls below the level of the battery supply. The switch switches to the main supply once its voltage level is above that of the battery supply.

For example, U.S. Patent 4,730,121 to Lee et al. describes one battery backup switching circuit which, in addition to the switching circuit, includes circuitry for receiving a reset or isolation signal. If the isolation signal is active, when the main power falls, the circuit will be isolated from both power sources.

U.S. Patent 5,315,549 to Scherpenberg et al. describes a memory controller which supplies backup battery power when the main power supply fails.

There are some logic elements, particularly those of the switching circuit and often other elements as well, which must continually receive some level of power. The switching circuit elements require the power in order to independently determine when the main power has returned. The other logic elements may require power in order to provide logic signals during battery power operation.

Unfortunately, the continually operative logic elements continually pull power from the battery, reducing the life of the battery. Accordingly, integrated circuit designers work to reduce the number of parts which utilize battery power.

It is possible that the part with the VLSI circuit will operate on battery power for a significant length of time, particularly when the part is stored in inventory, prior to be used for the first time. The battery might then be significantly rundown even before the part is ever utilized.

U.S. Patent 4,908,790 to Little et al describes a backup battery switching circuit which selectively connects the backup battery only when it is desired to preserve the data in the RAM. The microcomputer to which

the RAM is connected controls the switching circuit of Little et al and commands whether or not the backup battery is to be utilized.

SUMMARY OF THE PRESENT INVENTION

It is an object of the present invention to provide an improved backup battery switching circuit which utilizes the main power supply for as many elements as possible.

In accordance with a preferred embodiment of the present invention, in the switching circuit of the present invention, the comparator operates solely on the main power supply and provides a supply selection signal to two p-channel power transfer switches which separately transfer the battery and main power supplies to a single switched power supply node. To operate solely on main power, the comparator ensures that its selection signal is at a zero voltage level when the battery power supply should be selected and that the selection signal remains at the zero voltage level until the main power supply has a high enough voltage to properly activate standard CMOS (complementary metal-oxide semiconductors) elements.

Since the selection signal is low to indicate battery power, the battery power transfer switch is connected directly to the output of the comparator and the main power transfer switch is connected to an inverter which inverts the output of the comparator. The inverter operates on the battery supply in order to ensure that its output is a fully high signal during battery operation, thereby to completely shut off the main power transfer switch. This inverter draws no current during battery operation since, at that time, its input is forced to the zero voltage level.

Additionally, in accordance with a preferred embodiment of the present invention, the comparator includes a differential sense amplifier, a break before make switch and an override pull-down transistor, all of whom operate on the main power supply. The differential sense amplifier compares the voltage level of the main power supply with the voltage level of the battery power supply and produces a comparison signal. The break before make switch significantly separates any swings of voltage on the comparison signal and produces thereby the selection signal. The override pull-down transistor pulls the selection signal to a logic low value whenever the main power supply is below a predetermined minimum voltage level.

Moreover, in accordance with a preferred embodiment of the present invention, the switching circuit includes a low power sensing circuit which senses when the main power supply is below the minimum voltage level and provides an activation signal to the override pull-down transistor in response.

Further, in accordance with a preferred embodiment of the present invention, the switching circuit includes a diode between the battery power supply and

the p-channel battery power transfer transistor.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be understood and appreciated more fully from the following detailed description taken in conjunction with the drawings in which:

Fig. 1 is a general circuit diagram illustration of a backup battery switch, constructed and operative in accordance with a preferred embodiment of the present invention;

Fig. 2 is a circuit diagram illustration of a comparator, useful in the switch of Fig. 1;

Fig. 3 is a graphical illustration of an input signal utilized in the battery backup switch of Fig. 1;

Fig. 4 is a circuit diagram illustration of a circuit for producing an reclr signal, useful in the comparator of Fig. 2;

Fig. 5 is a block diagram illustration of a second backup battery switch, constructed and operative in accordance with a second preferred embodiment of the present invention, operative with a power up latch; and

Fig. 6 is a circuit diagram illustration of the power up latch of Fig. 5.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

Reference is now made to Fig. 1 which illustrates the backup battery switch 10 of the present invention within a VLSI circuit. Thus, Fig. 1 shows switch 10 receiving power from a main power supply 12 and from a battery 14 and providing a switched power supply signal, labeled V_{cco} , to a static random access memory (SRAM) array 16 and to other logic elements 17. The main power supply 12 supplies the main power signal V_{cc} and the battery 14 provides two supply signals, V_{stby} and V_{bat} . The backup battery switch 10 switches to the V_{bat} power supply when the variable voltage level of the main supply V_{cc} falls below the fixed voltage level V_{stby} of the battery.

It is noted that the V_{bat} signal is isolated from the battery 14 by a diode 18. This protects the battery 14 from possible shorting due to activity of the logic elements 17 and ensures that battery 14 does not receive an overvoltage when the main power supply V_{cc} rises higher than the battery power supply V_{bat} but the switch 10 has not yet switched to the main power supply V_{cc} .

The switch 10 comprises a comparator 20, having an output node 21, an inverter 22, a battery power transfer switch 24 and a main power transfer switch 26. Inverter 22 and power transfer switch 24 are both connected to node 21. The power transfer switches 24 and 26 are p-channel transistors (i.e. active low) whose output lines are connected together at node 32, thereby to

create switched power supply V_{cco} . The input to battery power transfer switch 24 is the V_{bat} power supply and the input to main power transfer switch 26 is the main power supply V_{cc} . Thus, V_{cco} will be equal to V_{cc} when main power transfer switch 26 is active and equal to V_{bat} when battery power transfer switch 24 is active.

Comparator 20 compares the voltage levels of the variable main supply V_{cc} with the fixed battery supply V_{stby} and, in accordance with a preferred embodiment of the present invention, operates solely on main power supply V_{cc} . To do so, comparator 20 ensures that its selection signal to node 21 is at a zero voltage if the battery supply V_{stby} is higher than the main supply V_{cc} and a high value otherwise. Comparator 20 also has a low power override circuit which forces the selection signal to stay at zero voltage for the entire period that the main power supply V_{cc} is below a minimum operating voltage V_{min} below which none of the CMOS elements of comparator 20 will work predictably. The minimum operating voltage V_{min} is typically higher than the sum of the threshold levels of the n-channel and p-channel transistors, each of which is typically 0.8V. Thus V_{min} is typically 1.8 - 2V.

Because of the polarity of node 21, battery power transfer switch 24 is controlled directly by node 21 and main power transfer switch 26 is controlled by inverter 22 which inverts the signal at node 21. Accordingly, a low value at node 21 activates battery power transfer switch 24 to provide the V_{bat} power supply to node 32. At the same time, the inverter 22 deactivates main power transfer switch 26, preventing the transfer of the V_{cc} power supply. The opposite is true for a high voltage level at node 21 which deactivates battery power transfer switch 24. The inverter 22 activates main power transfer switch 26 which, in turn, transfers the V_{cc} power supply to node 32.

It will be appreciated that operating comparator 20 on the main power supply V_{cc} minimizes the amount of battery power wasted for determining when to switch back to main power. It will further be appreciated that the inverter 22 must be operated on battery power V_{stby} to ensure that the power transfer switch 26 for the main power supply V_{cc} remains disconnected during battery operation. However, inverter 22 dissipates little power except for its direct leakage current. This is in contrast to the power dissipation of comparator 20 which, when active, utilizes significant amounts of power.

Reference is now made to Fig. 2 which details the elements of comparator 20. Comparator 20 comprises a differential sense amplifier 40, a capacitor 42, a break before make switch 44, an override pull-down transistor 49 and a driving buffer 46, all of whom operate on the main power supply V_{cc} .

The differential sense amplifier 40 is a standard differential sense amplifier biased by an "nbias" voltage and is well understood by those skilled in the art. The nbias voltage is a reference voltage close to the thresh-

old level V_{tn} of the n-channel transistors. It is created with a current source and an n-channel transistor operating as a diode.

Amplifier 40 produces a $stbyb$ signal which is high when the main power supply V_{cc} is high and low when the battery power supply V_{stby} is high. To minimize oscillations, amplifier 40 is a relatively low gain unit.

The capacitor 42 is connected to the line which carries the $stbyb$ signal and ensures that the $stbyb$ signal changes state relatively slowly. For example, if the V_{cc} supply is oscillating around voltage levels close to the V_{stby} supply, the capacitor 42 will smooth the oscillations.

The break before make switch 44, detailed hereinbelow, is a high gain circuit which amplifies the $stbyb$ signal ensuring that the output signal, called bat_onb , has significantly large swings to differentiate between the battery on state (when bat_onb is low) and the main power on state (when bat_onb is high). Since the voltage levels are significantly separated, the break before make switch 44 ensures that only one of the two power transfer switches 24 and 26 is activated at a time. By forcing the bat_onb signal to have large swings, break before make switch 44 helps to ensure that the bat_onb signal has a significantly low voltage level as the main power supply V_{cc} begins to fall below the battery power supply voltage level V_{stby} .

However, the break before make switch 44 only operates while the main power supply V_{cc} is above the minimum operating voltage V_{min} . For very low power operation, override pull-down transistor 49 maintains the bat_onb signal at a zero voltage value.

Override pull-down transistor 49 is active only while the voltage level of the main power supply V_{cc} is close to or below the minimum operating voltage V_{min} . For example, pull-down transistor 49 might be active until the main power V_{cc} achieves a voltage of 1.8V or 2V (by comparison, V_{stby} is 2.7V). While pull-down transistor 49 is active, it overrides the actions of differential sense amplifier 40 and break before make switch 44 (which are not working predictably due to the low voltage level of the main power supply V_{cc}) and forces the bat_onb signal to the zero voltage level. This maintains the high gain of comparator 20 even during very low power. Furthermore, during power up, pull-down transistor 49 protects against power-up glitches by maintaining the bat_onb signal at the zero voltage level until the main power supply V_{cc} has achieved a significant voltage level.

The buffer 46, comprised of two inverters 48, provides the strength to drive the p-channel transistor 24 since the exemplary break before make switch 44 has low current drive.

It will be appreciated that, due to the actions of break before make switch 44, the bat_onb signal has a zero voltage value shortly after the main power supply falls below the battery voltage level V_{stby} . Due to the override, pull-down transistor 49, the zero voltage value

is maintained while the main supply has low power. Thus, comparator 20 can operate properly on the variable main supply V_{cc} .

The operation of break before make switch 44 and pull-down transistor 49 will now be detailed.

The break before make switch 44 comprises two inverters 70 and 72 connected in series and a leaker transistor 74 connected to the first inverter 70 and controlled by the fixed n_{bias} signal. Each inverter, labeled "A" and "B" respectively, comprises a p-channel transistor 76 and an n-channel transistor 78.

Leaker transistor 74 limits the amount of current which can flow and forces the trip voltage at which the n-channel transistor 78A begins to conduct to be close to full V_{cc} level. Thus, when $stbyb$ has a voltage other than close to full V_{cc} , p-channel transistor 76A conducts and controls node 79, providing it with a high voltage level. When $stbyb$ has a voltage of close to V_{cc} , p-channel 76A is off and n-channel transistor 78A is on, pulling node 79 to towards ground. Node 79 thus swings between standard low and high voltage levels and thus, inverter 72 operates properly, providing the bat_onb signal with CMOS high and low voltage levels.

It will be appreciated that break before make switch 44 produces a high signal only once p-channel transistor 76A is fully shut off. Thus, break before make switch 44 ensures that the bat_onb signal is at a standard low voltage level whenever the main power supply 12 is close to or below the voltage level V_{stby} of the battery power supply 14.

As mentioned hereinabove, pull-down transistor 49 serves to override the actions of differential amplifier 40 and break before make switch 44, forcing the bat_onb signal to stay at the zero voltage level while the main power supply V_{cc} has too low a voltage level. This ensures that the bat_onb signal will be zero while the main power supply V_{cc} is off. Pull-down transistor 49 is connected between the bat_onb line and ground and is controlled by an $reclr$ signal.

Fig. 3, to which reference is now briefly made, illustrates the $reclr$ signal. As shown, the $reclr$ signal follows the voltage level of the main power supply V_{cc} until V_{cc} reaches a certain voltage level T, typically about 2V, which minimally is larger than V_{min} (e.g. equal to the combined threshold voltages of n-channel and p-channel transistors (each about 0.8V)). Above voltage level T, the $reclr$ signal drops back to a zero voltage level.

When the main power supply V_{cc} is fully on, the $reclr$ signal is inactive and pull-down transistor 49 does not affect the voltage of the bat_onb signal. As the main power supply V_{cc} drops below the voltage level T (i.e. when the CMOS transistors are no longer functioning reliably), the $reclr$ signal is activated, activating pull-down transistor 49 and forcing the voltage level of the bat_onb signal to zero. Furthermore, upon return of the main power supply V_{cc} , pull-down transistor 49 ensures that the bat_onb signal stays at zero until the main power supply V_{cc} is large enough, thereby preventing

glitches.

Reference is now briefly made to Fig. 4 which illustrates the circuit which produces the *reclr* signal. The circuit comprises a pull-up p-channel transistor 50, a leaker transistor 51, a capacitor 52, an inverter 53, a diode-connected n-channel transistor 54 and a second capacitor 55.

Diode-connected transistor 54 produces a relatively steady signal, *p_drv_psd*, whose voltage level is just above the threshold level V_{tn} of transistor 54. The signal *p_drv_psd* controls pull-up transistor 50 which receives, at its source, the main power supply V_{cc} . Its drain is connected to a node A which is also the source for leaker transistor 51, a small transistor which continually leaks a small current. Since the signal *p_drv_psd* is a low signal but not at the logic low level, pull-up transistor 50 begins to conduct only once its source is higher, by the amount of its threshold voltage V_{tp} , than its control signal *p_drv_psd* (which is at or close to V_{tn}). Thus, pull-up transistor 50 begins to conduct when V_{cc} is higher than $V_{tp} + V_{tn}$ (i.e. from 1.8V - 2V).

Inverter 53 inverts the level of node A, thereby producing the *reclr* signal. Thus, when the main power supply V_{cc} is below $V_{tp} + V_{tn}$, inverter 53 inverts the low level of node A to the V_{cc} level. However, since transistor 50 is physically much larger than leaker 51 (for example, transistor 50 might be of size 8/2.5 and leaker 51 of size 1/150), once pull-up transistor 50 conducts, it overcomes the effect of leaker 51 and relatively quickly changes node A to the level of the main supply V_{cc} . Inverter 53 then inverts the level of node A and produces a zero voltage signal. Thus, the *reclr* signal follows the voltage level of the main power supply V_{cc} until it reaches a threshold level T which, in this circuit is equal to $V_{tp} + V_{tn}$. Above voltage T, the *reclr* signal drops to the zero voltage level.

The transistors of the circuit of Fig. 4 typically have low leakage currents and, as such, do not respond quickly to rapid transitions of their input signals. Therefore, capacitors 52 and 55 are included to maintain node A and the *p_drv_psd* signal, respectively, at the desired voltage level during the rapid transition. Capacitor 52 couples node A to ground and capacitor 55 couples the *p_drv_psd* signal to the main power supply V_{cc} .

The circuit of Fig. 4 additionally shows two diode-connected n-channel transistors 56 which produce the control signal for leaker transistor 51 and transistors 57 which provide a resistance level to the circuit.

Reference is now made to Figs. 5 and 6 which illustrate an extension to the battery backup switch of Fig. 1. Fig. 5 is a block diagram of the entire backup battery circuit, including a first power up unit 75. Fig. 6 is a circuit diagram of a first power up latch 77 forming part of the power up unit 75.

In the embodiment of Fig. 5, the switched power supply V_{cco} is provided to the first power up unit 75 which passes the switched power supply V_{cco} , as sup-

ply V_{cco} , only if the main power supply V_{cc} has already been powered up once. Otherwise, no power is passed. As a result, when the part in which the circuit of Fig. 5 is incorporated is in inventory and not being used (which can be a significant portion of its lifetime), no battery power is provided to the SRAM 16 or to the logic elements 17. Battery power is provided, of course, to the elements of the backup battery switch 10.

It will be appreciated that the first power up unit 75 reduces the amount of battery power utilized during periods when the main power supply V_{cc} has not yet been activated. Thus, a part having the switch of Fig. 5 can be assembled with its battery and can be left in inventory for a significant length of time.

As shown in Fig. 5, the first power up unit 75 comprises a first power up latch 77 and a first power up transfer switch 79, wherein the first power up latch 77 controls the first power up transfer switch 79, only activating switch 79 when main power supply V_{cc} is applied for the first time. It is noted that the first power up latch 77 is powered by the switched V_{cco} signal and that first power up transfer switch 79 is a p-channel transistor.

Fig. 6 illustrates the elements of latch 77 which comprises a standard latch 80 utilizing the switched power supply V_{cco} and comprising three inverters 82, 84 and 86, a capacitor 88 and an input transistor 90. Input transistor 90 receives the *reclr* signal as input and is connected, on output, to a node 92. Node 92 is also connected to the output of inverter 82 and to the input of inverter 84. The output of inverter 84 is connected to a node 94 which is connected to the input of both inverters 82 and 86. Capacitor 88 is connected in parallel to node 94.

As mentioned hereinabove, the *reclr* signal follows the voltage level of the main power supply V_{cc} until a certain voltage level T above which the *reclr* signal drops back to a zero voltage level.

Before the main supply V_{cc} ever powers up, the switched signal V_{cco} carries either the battery supply V_{bat} or no supply if the battery has not yet been inserted. Since the *reclr* signal follows the main power supply V_{cc} , the *reclr* signal is at zero voltage and thus, the input transistor 90 is inactive. This remains true even during battery insertion since the *reclr* signal is a function of the main power supply V_{cc} and not of the switched power supply V_{cco} .

Once the battery has been inserted and switched power supply V_{cco} carries its voltage, latch 80 could carry any voltage value since its input signal (from transistor 90) is not yet defined. However, since capacitor 88 has not yet been charged, it will store any charge floating within the ring of inverters 82 and 84, thereby pulling node 94, to which it is connected, to a low level. Thus, latch 77 will produce a high output signal (since output inverter 86 inverts the value of node 94). Accordingly, first power up transfer switch 79 (Fig. 5) is inactive, thereby keeping the switched power signal V_{cco} away from the SRAM 16 and saving on battery power.

When main supply Vcc powers up, the voltage level of the reclr signal increases and, at one point, activates the input transistor 90. Since input transistor 90 is considerably larger than the p-channel transistor of inverter 82, the voltage drop across input transistor 90 pulls node 92 low. Inverter 84 inverts node 92, thereby making node 94 high. Because node 94 is high, the output of inverter 86, which is the output of the power up latch 77, is low, thereby activating first power up transfer switch 79.

As main supply Vcc continues to power up, the reclr signal returns to zero. However, this does not affect latch 77 since it does not change the low state of node 92. Thus, latch 77 maintains the correct state, continually providing a low signal to first power up transfer switch 79. Thus, first power up transfer switch 79 remains activated and the switched power signal Vcco continues to be transferred to the now activated SRAM 16 (Fig. 1).

It is noted that the n-wells of all of the p-channel transistors (Fig. 6) are powered by the Vcco source.

It will be appreciated by persons skilled in the art that the present invention is not limited to what has been particularly shown and described hereinabove. Rather the scope of the present invention is defined only by the claims which follow:

Claims

1. A comparator for a switching circuit which switches between a main power supply and a battery power supply and is connection on output to a selection line, the comparator operating on said main power supply, the comparator comprising:
 - a. a differential sense amplifier, operating on said main power supply, connected on input to said main power supply and to said battery power supply, for comparing the voltage level of said main power supply with the voltage level of said battery power supply and for producing a comparison signal;
 - b. a break before make switch, operating on said main power supply and connected on output to said selection line, for significantly separating any differences of voltage on said comparison signal and producing thereby a selection signal on said selection line; and
 - c. an override pull-down transistor, connected between said selection line and a ground supply and operative whenever said main power supply is below a predetermined minimum voltage level lower than the voltage level of said battery power supply, for forcing said selection signal to a logic low voltage value.

2. A switching circuit according to claim 1 and comprising a low power sensing circuit for sensing when said main power supply is below said predetermined minimum voltage level and for providing an activation signal to said override pull-down transistor in response.

3. A switching circuit for switching between a main power supply and a battery power supply, the switching circuit comprising:

- a. a comparator, operating on said main power supply, connected on input to said main power supply and to said battery power supply, for comparing the voltage level of said main power supply with the voltage level of said battery power supply and for providing a selection signal on a selection line, wherein said selection signal is low when said voltage level of said battery power supply is higher than said voltage level of said main power supply;

- b. a p-channel battery power transfer transistor controlled by said selection line for transferring said battery supply signal to a switched power supply node;

- c. an inverter, operating on said battery power supply and connected on input to said selection line, for inverting the voltage level of said selection signal; and

- d. a p-channel main power transfer transistor controlled by the output of said inverter for transferring said main power supply to said switched power supply node.

4. A switching circuit according to claim 3 and wherein said comparator comprises:

- a. a differential sense amplifier, operating on said main power supply, for comparing the voltage level of said main power supply with the voltage level of said battery power supply and for producing a comparison signal;

- b. a break before make switch, operating on said main power supply and connected on output to said selection line, for significantly separating any differences of voltage on said comparison signal and producing thereby said selection signal; and

- c. an override pull-down transistor, operative whenever said main power supply is below a predetermined minimum voltage level and connected between said selection line and a ground supply, for forcing said selection signal

to a logic low voltage value.

5. A switching circuit according to claim 4 and comprising a low power sensing circuit for sensing when said main power supply is below said predetermined minimum voltage level and for providing an activation signal to said override pull-down transistor in response. 5
6. A switching circuit according to claim 3 and also comprising a diode between said battery power supply and said p-channel battery power transfer transistor. 10

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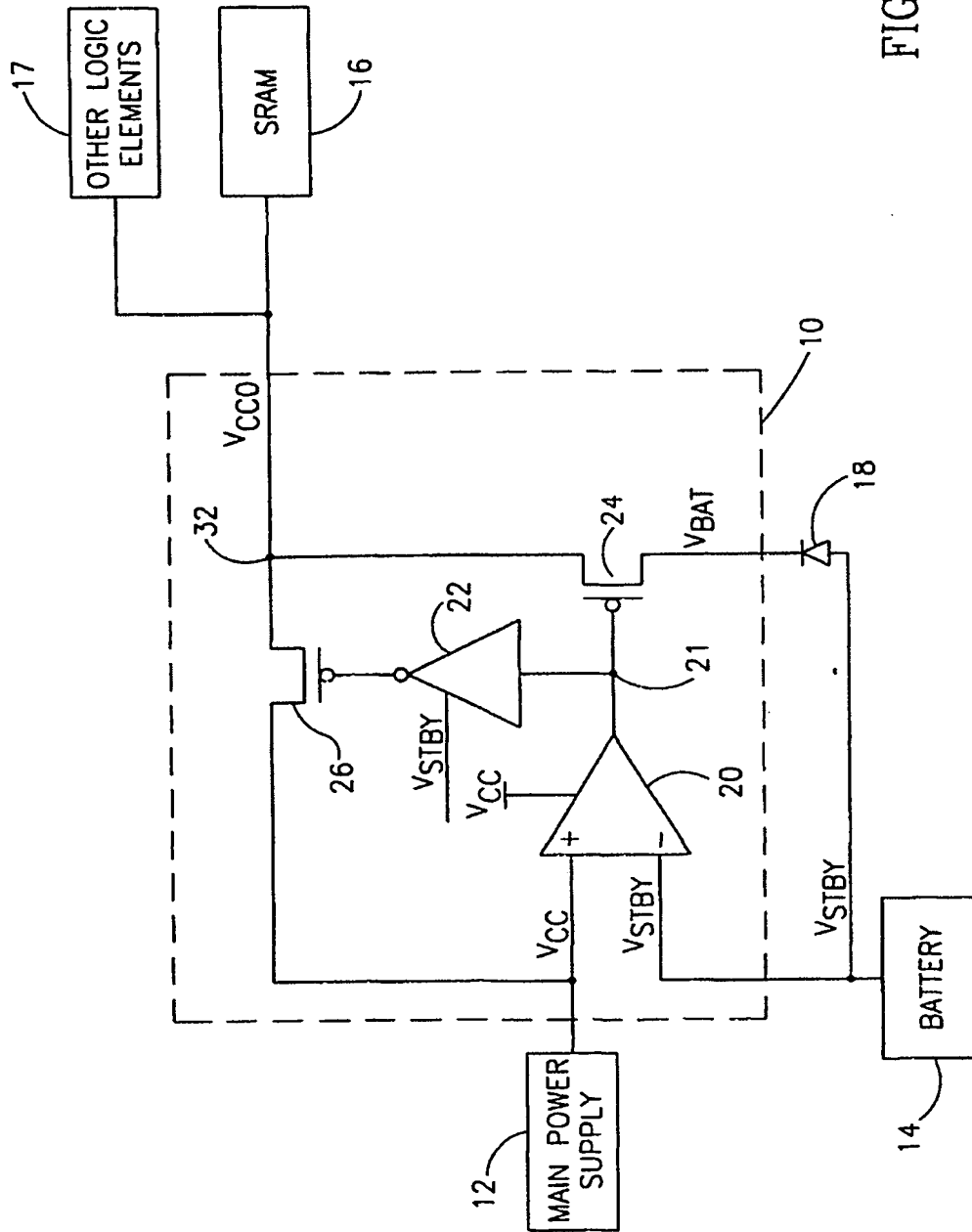
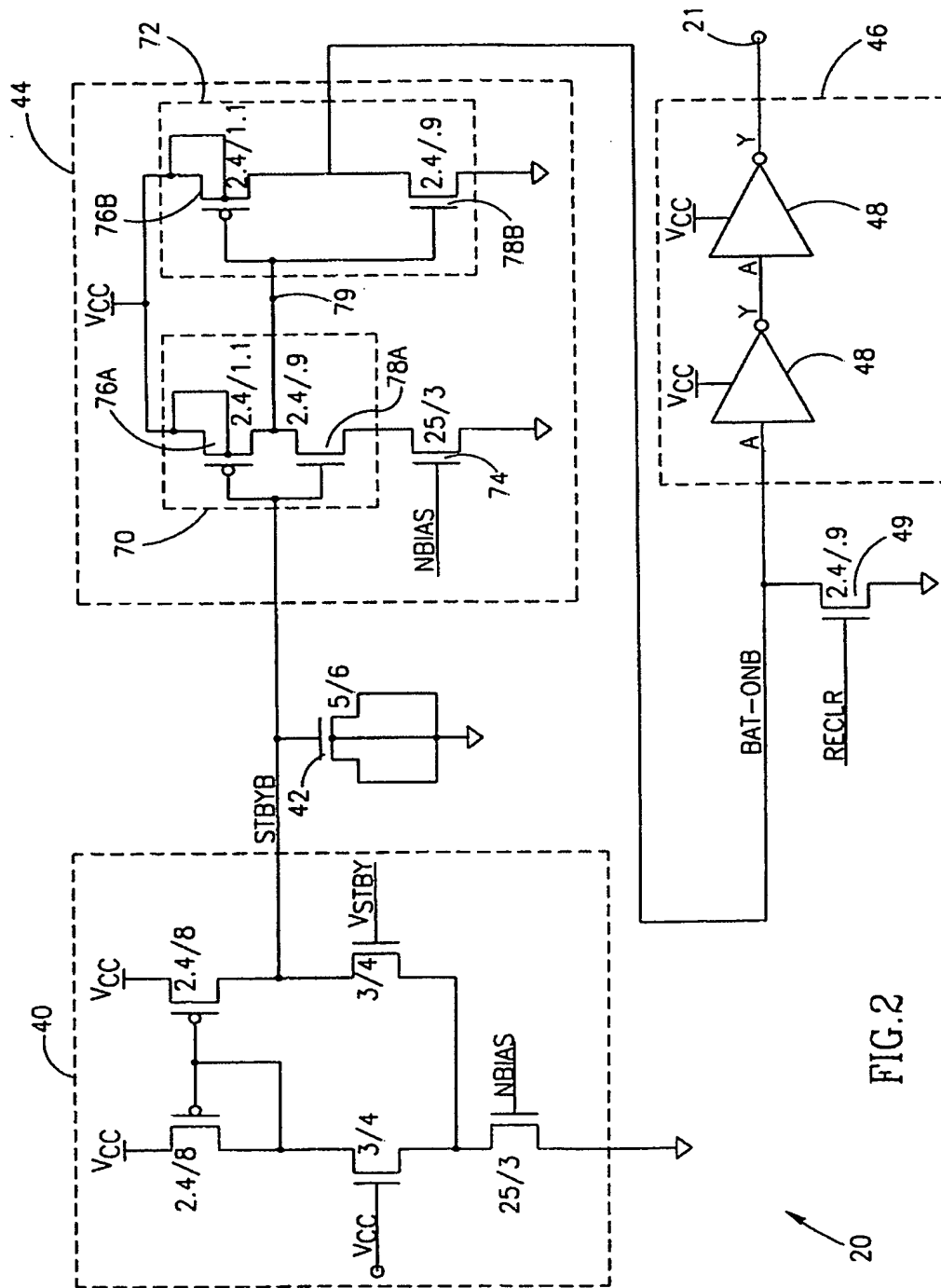
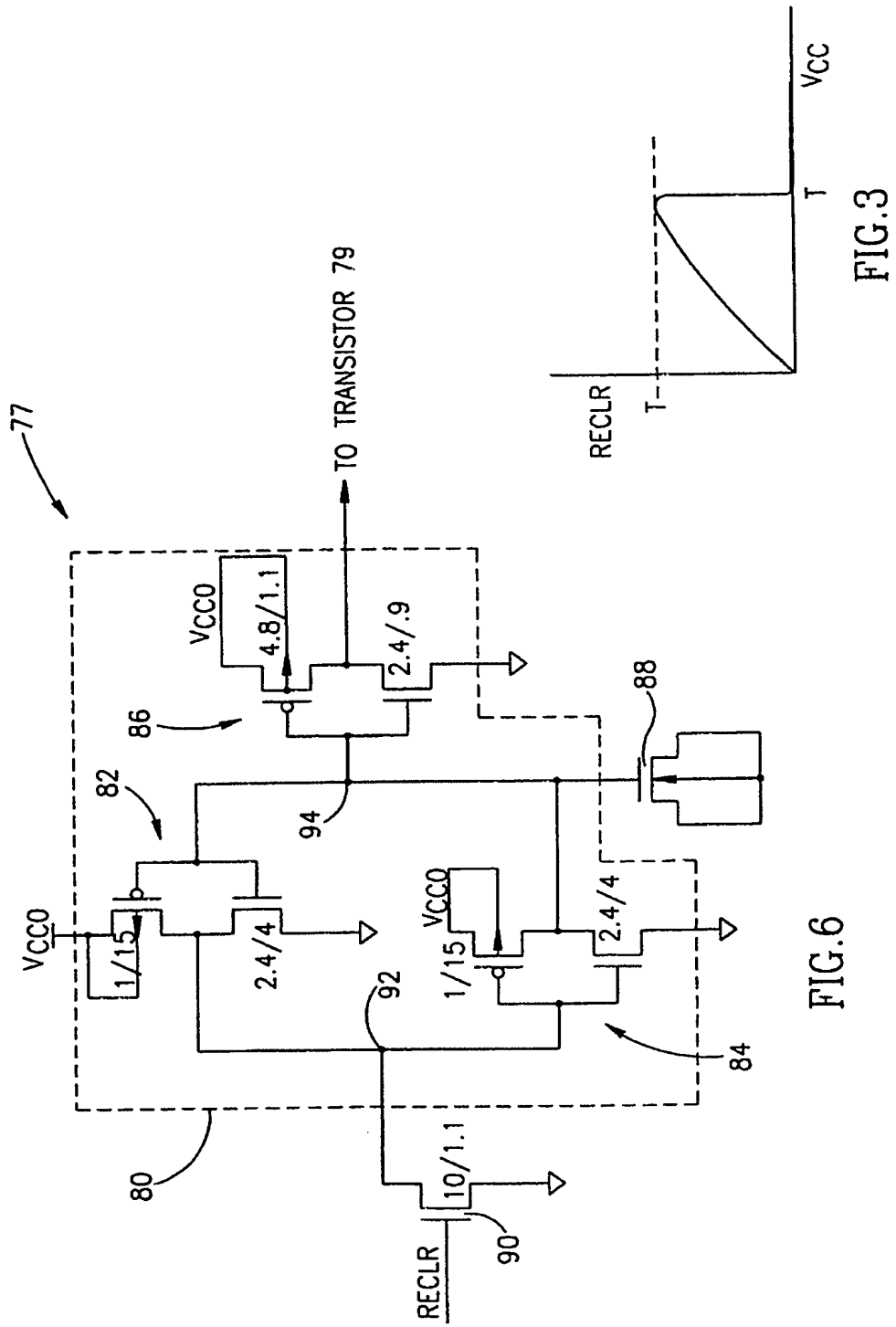


FIG. 1





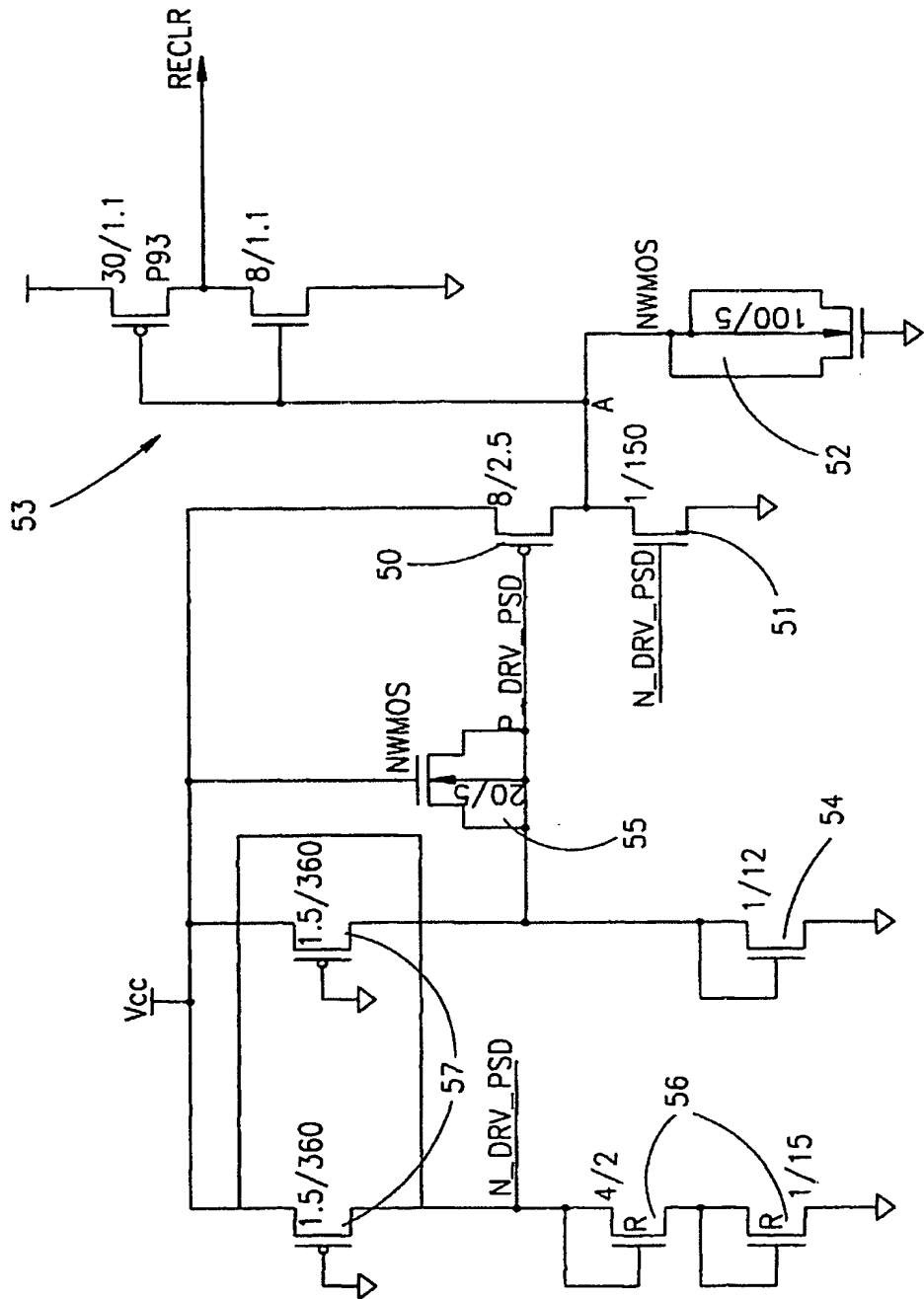


FIG. 4

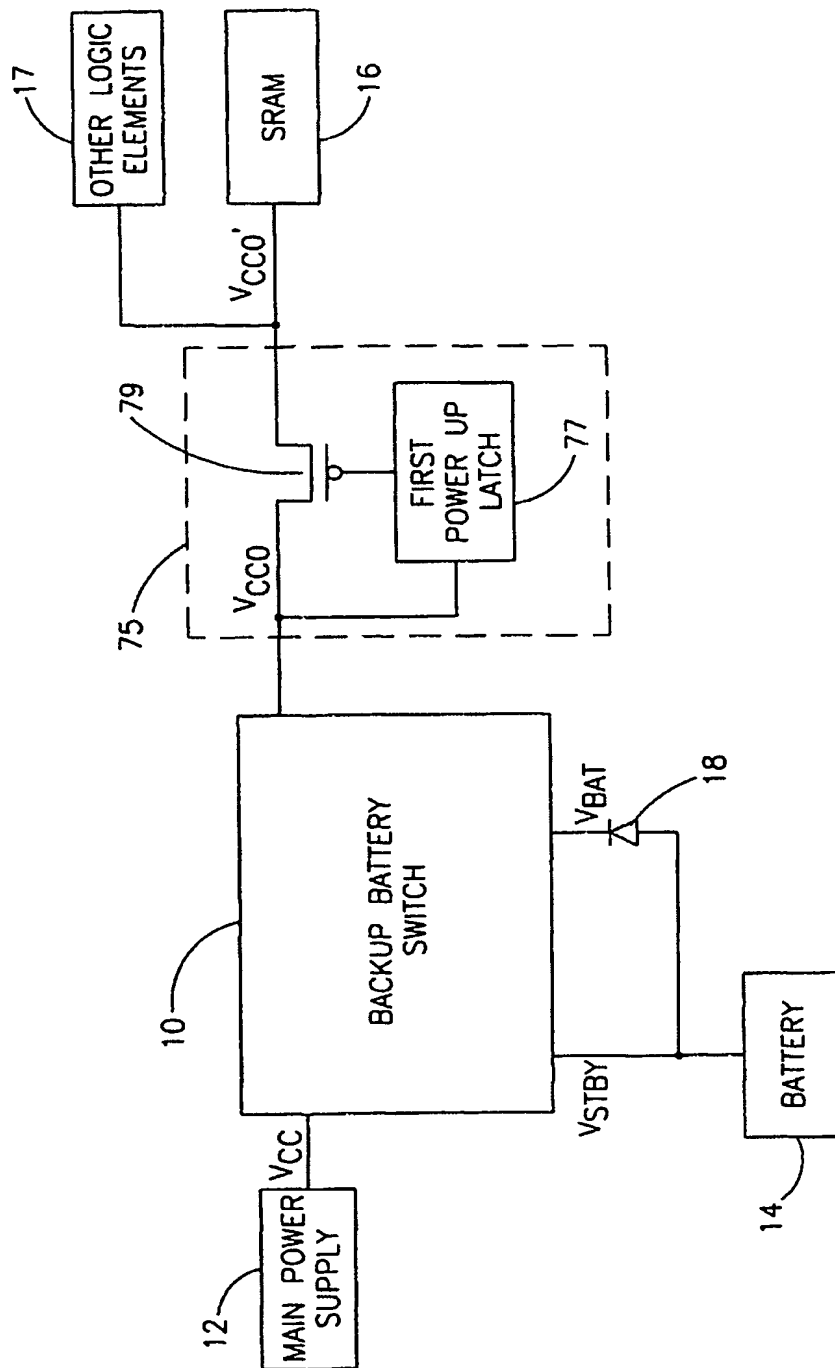


FIG. 5